Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A device for breaking leakage current path of a memory cell of a memory device, comprising:
a memory cell of a memory array, having a first bit line and a second bit line;
a first breaking circuit, connected between the first bit line of the memory cell and a power supplying terminal and between the second bit line and the power supplying terminal, wherein when the memory cell fails and in standby state, the first bit line and the power supplying terminal are disconnected, and the second bit line and the power supplying terminal are disconnected, by the first breaking circuit connected; and
a second breaking circuit, connected between the first bit line and a sense amplifier of the memory cell, and between the second bit line and the sense amplifier, wherein when the memory cell fails and in standby state, the first bit line and the sense amplifier are disconnected and the second bit line and the sense amplifier are disconnected by the second breaking circuit.

[c2] 2. The device of claim 1, wherein a word line of the memory cell is connected to the first breaking circuit.

[c3] 3. The device of claim 1, wherein a word line of the memory cell is connected to the second breaking circuit.

[c4] 4. The device of claim 1, wherein the second breaking circuit is comprised in the first breaking circuit.

[c5] 5. A method of breaking leakage current path of a memory cell of a memory device, comprising:
providing a first signal for disconnecting a connection between a first bit line and a power supplying terminal and disconnecting a connection between a second bit line and the power supplying terminal when a memory cell of a memory array fails and in standby state; and
providing a second signal for disconnecting a connection between the first bit line and a sense amplifier and disconnecting a connection between the second bit line and the sense amplifier.

[c6] 6. The method of claim 5, wherein the first signal is controlled by a word line of the memory cell.

[c7] 7. The method of claim 5, wherein the second signal is controlled by a word line of the memory cell.

[c8] 8. A memory device, comprising:
a memory array, having a plurality of memory cells, wherein each of the memory cells has a first bit line and

a second bit line;

a power supplying terminal, for providing power to the memory cells;

a sense amplifier;

a first breaking circuit, connected between the first bit line of the memory cell and the power supplying terminal, and connected between the second bit line and the power supplying terminal, wherein when at least one of the memory cell fails and in standby state, the first bit line and the power supplying terminal are disconnected, and the second bit line and the power supplying terminal are disconnected by the first breaking circuit connected; and

a second breaking circuit, connected between the first bit line and the sense amplifier of the memory cell, and between the second bit line and the sense amplifier, wherein when at least one of the memory cell fails and in standby state, the first bit line and the sense amplifier are disconnected and the second bit line and the sense amplifier are disconnected by the second breaking circuit.

[c9] 9. The memory device of claim 8, wherein a plurality of word lines of the memory cells are connected to the first breaking circuit.

[c10] 10. The memory device of claim 8, wherein a plurality of word lines of the memory cells are connected to the second breaking circuit.

[c11] 11. The memory device of claim 8, wherein the second breaking circuit is included in the first breaking circuit.

[c12] 12. The memory device of claim 8, wherein the memory array comprises a DRAM array.